Attorney Docket No.: SAM-0422

CLAIMS

What is claimed is:

1. A silicon-on-insulator (SOI) wafer comprising:

a first semiconductor wafer including an isolation insulating film formed to define an active region;

a well region and a buried layer formed in the active region of the first semiconductor wafer; and

a second semiconductor wafer bonded with the first semiconductor wafer, wherein an SOI insulating film, which contacts a lower portion of the isolation insulating film and electrically insulates a lower portion of the active region, is formed.

- 2. The SOI wafer of claim 1, wherein the isolation insulating film is a trench-shaped silicon oxide film.
 - 3. The SOI wafer of claim 1, wherein the well region and the buried layer form

an NMOS region and a PMOS region, respectively.

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- 4. The SOI wafer of claim 3, wherein a P-well is formed in the NMOS region, and an N-well is formed in the PMOS region.
- 5. The SOI wafer of claim 1, wherein the SOI insulating film is a silicon oxide film.
 - 6. The SOI wafer of claim 1, wherein the first semiconductor wafer provides the active region, and wherein the second semiconductor wafer comprises a support wafer that supports the first semiconductor wafer.

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- 7. A method of manufacturing an SOI wafer, the method comprising:
- a) forming an isolation insulating film on a front face of a first semiconductor wafer to define an active region and forming a bonding insulating film on a front face of a second semiconductor wafer;
- b) performing an ion implantation process so as to form a P-well and an N-well in the active region;

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- c) pre-bonding the respective front faces of the first semiconductor wafer and the second semiconductor wafer;
- d) heating the bonded first and second semiconductor wafers at a predetermined temperature to completely bond the first and second semiconductor wafers with each other; and
- e) polishing a back face of the first semiconductor wafer to a bottom level of the isolation insulating film.
- 8. The method of claim 7, wherein step a) comprises:
 forming a mask insulating film on the surface of the first semiconductor wafer;
 forming an isolation trench on the mask insulating film and the first
 semiconductor wafer;

forming a trench fill insulating film so as to bury the isolation trench; and planarizing the trench fill insulating film to a level of the mask insulating film using a planarization process.

- 9. The method of claim 8, wherein the mask insulating film includes a silicon oxide film.
- 10. The method of claim 9, wherein the mask insulating film further includes a silicon nitride film.
- 11. The method of claim 8, wherein the trench fill insulating film is a silicon oxide film.

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12. The method of claim 8, wherein chemical mechanical polishing (CMP) is used in the planarization process.

- 13. The method of claim 7, wherein in step a), the bonding insulating film is a silicon oxide film.
- 14. The method of claim 13, wherein the bonding insulating film is formed by thermally oxidizing the substrate silicon of the second semiconductor wafer.
- 15. The method of claim 7, wherein step b) comprises: forming a photoresist having a pattern with which a region in which an N-well

is to be formed is opened, on the first semiconductor wafer;

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implanting N-type impurities in the substrate silicon of the first semiconductor wafer using ion implantation and using the patterned photoresist as a mask; and removing the photoresist.

16. The method of claim 8, wherein step b) comprises:

forming a photoresist having a pattern with which a region in which a P-well is to be formed is opened, on the first semiconductor wafer;

implanting P-type impurities in the substrate silicon of the first semiconductor wafer using ion implantation and using the patterned photoresist as a mask; and removing the photoresist.

- 17. The method of claim 16, wherein the N-type impurities are 5-valence electron ions, including phosphorus (P), arsenic (As), and antimony (Sb).
- 18. The method of claim 16, wherein the P-type impurities are 3-valence electron ions, including boron (B) and BF₂.

19. The method of claim 7, wherein step c) comprises: arranging the first and second semiconductor wafers so that their respective front faces are adjacent each other; and

vertically applying a force to a back face of a bonded surface of the first and second semiconductor wafers.

- 20. The method of claim 19, wherein step c) further comprises absorbing certain H₂O vapor into the surfaces at which the first and second semiconductor wafers are bonded with each other.
- 21. The method of claim 7, wherein step d) is performed at a temperature higher than a temperature at which ions implanted in the N-well and the P-well form a well.
- 22. The method of claim 7, wherein step e) comprises:

 preparing a back face of the first semiconductor wafer to be a polishing face; and

polishing substrate silicon on the back face of the first semiconductor wafer using a polishing process.

- 23. The method of claim 22, wherein polishing the substrate silicon comprises grinding the back face of the first semiconductor wafer using a grinder.
- 24. The method of claim 22, wherein chemical mechanical polishing (CMP) is used as the polishing process.
 - 25. The method of claim 24, wherein in the polishing process, the isolation insulating film is used as a polishing stopper.

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26. The method of claim 7, after step e), further comprising forming a protection insulating film on a top surface of a semiconductor substrate.

27. The method of claim 26, wherein the protection insulating film is a silicon oxide film.

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